Curriculum Vitae et Studiorum

Alessandro De Laurenzis

Bari (Italy), 22nd September 1971

Contacts

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Carrier objectives

Providing quality solutions to semiconductor design problems within scope and tight schedules. Extensive experience in ASIC implementation and digital design methodologies. Flexible as regards moving from project to project. Proven team technical leadership skills. Now looking to continue making a significant contribution within similar environments (consultancy role or permanent position).

Job experiences

Sep 2015 – Now

STMicroelectronics (Castelletto Design Center, Milano, Italy)
AMG – Analog & MEMS Group
MSD – MEMS Sensors Division

Hardware Design Project Mgr. – Physical Design & Signoff Leading

Physical implementation and verification of core logic for MEMS inertial modules (accelerometers, gyroscopes, microphones, environmental sensors):

- RTL to GDS-II flow (RTL analysis, constraints definition, logic synthesis, DFT, formal verification, PnR, timing and power analysis, DRC/LVS);
- 130nm std CMOS technology;
- Ultra-low-power design (with very-low-area target);
- Strict cooperation with test engineering team, PDK and design platform internal suppliers;
- Digital CAD flows adoption and consolidation.

Extensive use of *Synopsys, Cadence* and *Mentor Graphics* CAD tools:

- *Design Compiler*, *SpyGlass*, *Formality*, *StarRC*, *PrimeTime*, *TetraMAX*;
- *Innovus* / *EDI* Implementation System;
- *Calibre* IC Physical Verification (DRC, LVS, DESIGNrev).

Nov 2011 – Sep 2015

STMicroelectronics (Castelletto Design Center, Milano, Italy)
DCG – Digital Convergence Group
DAP – Digital ASIC Products / HSI – High Speed Interfaces

Hardware Design Project Mgr. – Physical Design Team Leader

Digital implementation and top-level integration of mixed-signal IPs (Ethernet PHY and SerDes):

- RTL to GDS-II flow (flip-chip packaging co-design, P&R, STA, formal verification, DRC/LVS, DFM);
- DSM std CMOS technologies (32/28nm, bulk and FDSOI);
- Low power design within tight area/congestion constraints (EPHY);
- High frequency (up to 28GHz) multi-voltage environments (SerDes);
- Library distribution: IP logic/physical views preparation (following internal maturity level standards) and packaging (ST UniCAD MAT10).

Job experiences

May 2010 – Nov 2011 ***PEGASUS Microdesign***

Digital IC Design and Implementation Specialist

Nov 2010 – Nov 2011 On-site resident **BE designer** at:
Accent (Vimercate office, Milano, Italy)

RTL to GDS-II flow (including constraints definition, topographical synthesis, P&R, STA, physical verification)

- mixed-signal environments;
- DSM std CMOS technologies (by TSMC, GSMC);
- medium-to-high complexity SoC/SiP (smart grid power line controllers).

May 2010 – Nov 2010 On-site resident **DFT engineer** at:
STMicroelectronics (Castelletto Design Center, Milano, Italy)
CCI – Computer & Communication Infrastructure product group
CSD – Computer Systems Division / Digital Design Team

Design, implementation and verification of testability features for high-volume production SoC/CSSP (SPEAr family)

- 55 nm low-power CMOS technology;
- 6.5 MGate / 500 MHz;
- scan architecture for multi-model faults detection (SSAF, TF), at-speed testing (OCC insertion and hierarchical recognition), test patterns validation, BSD/JTAG interfaces.

Jun 2009 – May 2010 ***MAYA Technologies***

Digital IC Design and Implementation Specialist

On-site resident consultant at:
ST-Ericsson (Grenoble Design Center, France)
WMM – Wireless MultiMedia Division

Front-to-back-end design flows for low-power wireless communication IPs (imaging accelerators for multimedia mobile processors, Nomadik family)

- 45-40 nm low-power CMOS technologies;
- up to 1.5 MGate / 500 MHz;
- constraints definition, logic synthesis, DFT insertion, ATPG, formal verification, sign-off STA support.

May 2008 – Jan 2009 ***ESTEREL EDA Technologies***

Digital IC Design and Implementation Specialist

On-site resident consultant at
Texas Instruments (Nice Design Center, France)
WTBU – Wireless Terminal Business Unit

Ultra-low-power multi-voltage clock distribution networks synthesis for wireless communication IPs (3.5G smart-phone modems):

- 65 nm low-power CMOS technology;
- 1.5 MGate / 200 MHz;
- power-aware clock tree planning;
- advanced clock-gating optimization techniques (*Azuro* ***PowerCentric***), complex non-default routing rules definition, timing closure (*Magma* ***Talus***) and STA (*Synopsys* ***PrimeTime***).

Job experiences

May 2004 – May 2008

STMicroelectronics (Napoli Design Center, Italy)
CPG – Computer Peripherals Group
CSD – Computer Systems Division / Chip Assembly Team

Digital ASIC Designer (Physical Implementation Expert)

Chip level design of printer digital engines, re-configurable connectivity systems and PC south-bridges (including back-end flows, SoC integration and development of innovative design methodologies and solutions in cooperation with R&D teams):

- deep sub-micron standard and low-power CMOS technologies (130, 90, 65 nm);
- up to 5 MGate / 500 MHz;
- constraints definition, logic synthesis, DFT (scan chains insertion & reordering), formal verification;
- floor-planning, physical synthesis, complex clock trees management;
- MMMC timing closure;
- DFM (antenna fixing, metal dummy insertion, metal line spreading, resolution enhancement rules), signoff STA, physical verification.

Feb 2001 – May 2004

STMicroelectronics (Castelletto Design Center, Milano, Italy)
CPG – Computer Peripherals Group
DSD – Data Storage Division / R/W Channel Design Group

Digital and Mixed-Signal ASIC Designer

Integration of small and very fast digital blocks (control logic for PLLs and ADCs, serial/parallel interfaces, synchronization circuits) in the analog circuitry of computer peripherals (read/write channels for hard disk drives):

- deep-sub-micron standard CMOS technologies (180-130 nm);
- up to 100 kGate, 1.8 GHz;
- spec to GDS-II flow: RTL description, schematic capture, synthesis, timing closure, sign-off checks.

Jul 2000 – Feb 2001 ***C.E.C.*** *– Concurrent Engineering Consulting*
Altran Group (Milano, Italy)

Consultant Engineer

On-site resident at:
Magneti Marelli S.p.A. (Corbetta, Milano, Italy)
Divisione Sistemi Elettronici

Firmware & software programming - Real-time embedded systems for automotive industry (car dashboards):

- MCU: Motorola MC68HC11/08, NEC iPD78F0828;
- C coding, lab testing.

Apr 2000 – Jul 2000 ***Pool Consulting*** – Altran Group (Torino, Italy)

Consultant Engineer

Electronic system reliability and fault analysis (in co-operation with ***Alenia Difesa DSAE***, Torino, Italy)

Curriculum Vitae et Studiorum

Languages

Italian mother-tongue
Fluent **English**, basic **French**

Education

Oct 1990 – Feb 2000 — ***Polytechnic of Bari*** (Bari, Italy)

University degree in **Electronics Engineering** (MSEE-equivalent), specializing in **Microelectronics**, got with **full marks *cum laude***.

Graduation thesis in **Electronic Technologies and Materials**: "*New-generation electro-optic modulators: a technological processing review*" - Main topics: technological processing of 3-dimensional optical confinement structures (proton exchange and metal diffusion in LiNbO3 substrates for refraction index modification, chemical dry and wet etching for geometry definition); mathematical models (based on diffusion kinetics) correlating optical wave-guides properties with process conditions; realization, characterization and testing of wave-guides suitable for very high speed electro-optic modulators.

Other essays:

- *Data-flow systems: graphs, languages and architectures* (**Computer architecture**, Dec 1996);
- *Planar dielectric waveguides index profile reconstruction: IWKB techniques* (**Optoelectronics**, Nov 1997);
- *Transferred-electrons oscillators (TEO): fundamentals & performance analysis* (**Electronic Technologies and Materials**, Feb 1998);
- *Built-in approach for testing of complex digital circuits* (**Computer-aided design of electronic circuits and systems**, Sep 1998).

Sep 1985 – Jul 1990 — *"**Giulio Cesare**"* secondary school (Bari, Italy)

Accountancy and Computer Programming Certificate of Education obtained with **full marks**

Additional training

Sep 2004 (3 days) — ***Synopsys Italia*** – Customer Education Services (Agrate Brianza, Milano, Italy)

***Astro* Workshop**

May 2003 (5 days) — ***Mentor Italia*** – *Customer Training Center* (Milano, Italy)

VHDL Syntax using *Advance MS*

Apr 2001 (5 days) — ***Synopsys Italia*** – Customer Education Services (Agrate Brianza, Milano, Italy)

***Chip Synthesis* and *Physical Compiler* Workshops**

May 2000 (10 days) — ***Pool Consulting*** – Altran Group (Torino, Italy)

RAMS Techniques: Reliability, Availability, Maintainability and Safety analysis in the industrial standards; FMEA and FMECA.

Technical skills

Proficiency in SoC/ASIC digital design methodologies and implementation CAD flows within leading-edge CMOS technologies: RTL analysis, top- and block-level constraint management, logic and physical synthesis, DFT insertion, low-power CTS, STA, power analysis, physical verification); hands-on experience with multiple EDA vendor tools:

- *Synopsys*: Galaxy Design Platform (***Design Compiler***, ***DC Explorer***, ***DFTMAX***, ***TetraMAX***, ***IC Compiler***, ***StarRC***, ***PrimeTime***);
- *Cadence*: ***Innovus / EDI*** digital implementation, ***Conformal*** (LEC, ECO, LP), ***Incisive*** Enterprise Simulator, ***Virtuoso*** custom IC suites;
- *Mentor Graphics*: ***Calibre*** IC physical verification, analog & mixed-signal verification (***Eldo***, ***ADMS***).

Solid knowledge of low-power design techniques (advanced clock gating, multi-Vt libraries usage, multi-voltage design, adaptive voltage scaling), deep-sub-micron effects (aging, temperature inversion, on-chip variability, leakage, wire-length distribution, pin capacitance variation, ESD, latch-up), signal integrity (IR-drop, cross-talk, electro-migration), multi-clock-domain designs and synchronization circuits (hand-shake protocols, circular registers, FIFOs).

Good understanding of Unix/BSD/Linux environments, scripting (***Tcl***, ***sh***), hardware description languages (***Verilog***, ***VHDL***), general-purpose programming languages (***C***, ***Pascal***).

Basics of feasibility studies & chip size estimation, packaging, bonding, I/O ring definition, MCU architectures, standard interfaces (UART, Ethernet, USB, SPI, I2C/I3C).

Military status

Liability to military service accomplished in 1999

Personal skills

Strong willingness to work in a challenging environment.

Self-motivation, pro-activity, determination and perseverance to achieve targets.

Team-working; flexibility and adaptability; ability to work under intensive pressure to meet strict deadlines.

Personal notes

Marital status: Single

Hobbies: Modern and contemporary art, sport (biking, trekking), rock and pop music, astronomy, photography.

Reading: Novels, strip cartoon stories, fiction, essay, fantasy, detective stories, contemporary history.

References may be furnished upon request.